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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,452	09/26/2001	Andrew Marshall	TI-28975	5345

23494 7590 12/03/2003

TEXAS INSTRUMENTS INCORPORATED
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DALLAS, TX 75265

EXAMINER	
TANG, MINH NHUT	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,452	MARSHALL ET AL.	
	Examiner	Art Unit	
	Minh N. Tang	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 5, it is not clear "at least one global input" applied to which element. For examination purposes, the limitation "in dependence on at least one global input" is interpreted as -- in dependence on at least one global input applied to said probe pad --.

Claims 6-8 are rejected since they depend on rejected base claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freed (U.S.P. 3,781,683) in view of Hubacher (U.S.P. 3,849,872).

As to claims 1 and 3, Freed discloses, in Fig. 2, a partially fabricated wafer, comprising: at least one probe pad (30-38); multiple test structures (i.e., odd and even testing circuits repeatedly formed in the kerf, hereafter testing circuits) which are selectably multiplexed (i.e., transmitting signals through testing circuits) to said probe pad (30-38). Freed does not explicitly disclose applying a voltage to probe pad (30-38). Hubacher discloses, in Figs. 1 and 2, a test system for selectively activating a chip (35) comprising a transistor (25) formed in the wafer kerf having a base (29), a collector (28) and an emitter (30), a voltage signal (+V) being applied to the collector (28) and a simultaneous signal being applied to the base (29) of the transistor (25), respectively, in order to select a particular transistor for producing a higher voltage output on the emitter (30). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the apparatus of Freed by providing an appropriate voltage to the collector and the base of the transistor (i.e., pad 31, pad 37 connected to collector and base of transistor T2 in Freed reference) as taught by Hubacher so that a corresponding voltage would produce at the emitter of the transistor.

As to claims 2, 6 and 10, Freed discloses in Fig. 2, said probe pad (30-38) is located in a scribeline (vertical kerf 11), and occupies more than half (see, for example pads 36, 38) the width of said scribeline (11).

As to claims 4, 8 and 11, Freed in view of Hubacher disclose said multiple test structures (testing circuits) are selectively multiplexed to said probe pad (30-38) in dependence on sequence of voltages (i.e., voltage applied to the collector and the base of the transistor T2) applied to said probe pad (30-38).

As to claims 5 and 7, Freed discloses, in Figs. 2 and 3, a partially fabricated wafer including die (10) separated by scribelines (11, 12), comprising: at least one probe pad (30-38) in a scribeline (11); multiple test structures (i.e., odd and even testing circuits repeatedly formed in the kerf, hereafter testing circuits) in said scribeline (11) which are all physically close to said probe pad (30-38), and which are selectably multiplexed (i.e., transmitting signals through testing circuits) to said probe pad (30-38). Freed does not explicitly disclose applying at least one global input to said probe pad (30-38). Hubacher discloses, in Figs. 1 and 2, a test system for selectively activating a chip (35) comprising a transistor (25) formed in the wafer kerf having a base (29), a collector (28) and an emitter (30), a voltage signal (+V) being applied to the collector (28) and a simultaneous signal being applied to the base (29) of the transistor (25), respectively, in order to select a particular transistor for producing a higher voltage output on the emitter (30). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the apparatus of Freed by providing an appropriate voltage to the collector and the base of the transistor (i.e., pad 31, pad 37 connected to collector and base of transistor T2 in Freed reference) as taught by Hubacher so that a corresponding voltage would produce at the emitter of the transistor.

As to claims 9 and 12, Freed discloses, in Figs. 2 and 3, a scribeline test circuit, comprising: a test selector circuit (T2) located in a single scribeline portion (kerf 11) between two adjacent die locations (i.e., between dice 10); multiple test structures (i.e., odd and even testing circuits repeatedly formed in the kerf, hereafter testing circuits), also located in said single scribeline portion (11); and at least one probe pad (30-38), also located in said single scribeline portion (11); wherein said test selector circuit (T2) makes an electrical connection from said probe pad (30-38) only to a selected one (i.e., odd testing circuit) of said test structures (testing circuits). Freed does not explicitly disclose applying a voltage at said probe pad (30-38). Hubacher discloses, in Figs. 1 and 2, a test system for selectively activating a chip (35) comprising a transistor (25) formed in the wafer kerf having a base (29), a collector (28) and an emitter (30), a voltage signal (+V) being applied to the collector (28) and a simultaneous signal being applied to the base (29) of the transistor (25), respectively, in order to select a particular transistor for producing a higher voltage output on the emitter (30). It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the apparatus of Freed by providing an appropriate voltage to the collector and the base of the transistor (i.e., pad 31, pad 37 connected to collector and base of transistor T2 in Freed reference) as taught by Hubacher so that a corresponding voltage would produce at the emitter of the transistor.

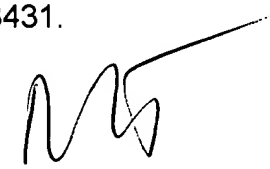
Conclusion

6. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (703) 305-1652. The examiner can normally be reached on M-F (6:30-4:00) first Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mrs. Cuneo, Kamand can be reached on (703) 308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-3431.



Minh Tang
November 19, 2003